In the Claims:

1. (Original) A semiconductor wafer having an asymmetric edge profile (EP) extending between an inner edge profile (EP_{in}) and an outer edge profile (EP_{out}) as illustrated by FIG. 1, which is incorporated herein;

wherein t is a thickness of the semiconductor wafer, ϕ_1 is an angle in a range between about 30° and about 85°, R is a radius of an arc that defines EP_{in} at a point of intersection with a top surface of the semiconductor wafer, and α is an acute angle that represents an angle of intersection between a bottom surface of the semiconductor wafer and a line that is tangent to the arc at a point on EP_{out}; and

wherein:

$$A_1=R(1-\cos\phi_1);$$

$$A_2=R(1-\sin\alpha) + (t-R\sin\phi_1 - R\cos\alpha)\cot\alpha;$$

$$B_1=R\sin\phi_1; \text{ and}$$

$$B_2=t-R\sin\phi_1.$$

2. (Original) The wafer of Claim 1, wherein R is in a range between about 0.23t and about 0.5t.

3. (Original) The wafer of Claim 2, wherein A_2 is greater than about two times A_1.

4. (Original) The wafer of Claim 2, wherein ϕ_1 is in a range between about 60° and about 75°.

5. (Original) The wafer of Claim 2, wherein t is in a range between about 625 μm and about 825 μm.

6. (Currently amended) A semiconductor wafer having an asymmetric edge profile (EP) extending between an inner edge profile (EP_{in}) and an outer edge profile (EP_{out}) as illustrated by FIG. 1, which is incorporated herein; wherein ϕ_1 is an angle in a range between about 30° and about 85°; and wherein R is in a range between about 0.23t and about 0.5t, where t is a thickness of the semiconductor wafer.

7. (Original) The wafer of Claim 6, wherein A_2 is greater than about two times A_1.

8. (Original) The wafer of Claim 6, wherein ϕ_1 is in a range between about 60° and about 75°.

9. (Original) The wafer of Claim 6, wherein t is in a range between about 625 μm and about 825 μm.

10. (Currently amended) A semiconductor wafer having an asymmetric edge profile (EP) extending between an inner edge profile (EP_{in}) and an outer edge profile (EP_{out}) as illustrated by FIG. 1, which is incorporated herein, where ϕ_1 is an angle in a range between about 30° and about 85°.

11.-17. (Canceled)

18. (Currently amended) A semiconductor wafer having an asymmetric edge profile (EP2) extending between an inner edge profile ($EP2_{in}$) and an outer edge profile ($EP2_{out}$) as illustrated by FIG. 2, which is incorporated herein; wherein ϕ_1 and ϕ_2 are angles in a range between about 30° and about 85° ; wherein $\phi_1 < \phi_2$; and wherein R is in a range between about 0.23t and about 0.5t, where t is a thickness of the semiconductor wafer.

19. (Original) A semiconductor wafer having an asymmetric edge profile (EP2) extending between an inner edge profile ($EP2_{in}$) and an outer edge profile ($EP2_{out}$) as illustrated by FIG. 2, which is incorporated herein;

wherein t is a thickness of the semiconductor wafer, ϕ_1 is an angle in a range between about 30° and about 85°, ϕ_2 is greater than ϕ_1 and less than about 85°, R is a radius of an arc that defines $EP2_{in}$ at a point of intersection with a top surface of the semiconductor wafer, and α is an acute angle that represents an angle of intersection between a bottom surface of the semiconductor wafer and a line that is tangent to the arc at a point on $EP2_{out}$; and

wherein:

$$A_1=R(1-\cos\phi_1);$$

$$A_2=R(1-\sin\alpha) + (B_2 - R\cos\alpha)\cot\alpha;$$

$$B_1=R\sin\phi_1; \text{ and}$$

$$B_2=t-R\sin\phi_1.$$

20. (Canceled)